WHAT IS CLAIMED IS:

1. A thin film transistor array substrate for a liquid crystal display, the thin film transistor array substrate comprising:

a plurality of gate lines formed at a transparent insulating substrate;

a plurality of data lines insulatively crossing over the gate lines to define pixel regions;

common electrodes at the pixel regions; pixel electrodes at the pixel region spaced apart from the common electrodes with a predetermined distance;

thin film transistors, each of which has a semiconductor pattern; and

a light interception pattern formed of same material as the semiconductor pattern.

2. The thin film transistor array substrate of claim 1, wherein the light interception pattern is overlapped with the corresponding data line, and the common electrode or the pixel electrode close to the corresponding data line.

3. The thin film transistor array substrate of claim 1, wherein the light interception pattern is overlapped with the common electrode or the pixel electrode of the neighboring pixel regions.

4. The thin film transistor array substrate of claim 1, wherein the semiconductor pattern is connected to the corresponding light interception pattern.

5. The thin film transistor array substrate of claim 1, wherein the semiconductor pattern is extended to the bottom of the corresponding data line.

6. The thin film transistor array substrate of claim 1, wherein the light interception pattern is extended external to the periphery of the corresponding data line.

7. The thin film transistor array substrate of claim 1, wherein the common

electrodes are formed at the same plane as the gate lines.

8. The thin film transistor array substrate of claim 1, wherein the pixel electrodes are formed at the same plane as the data lines.

9. The thin film transistor array substrate of claim 1, wherein the pixel electrodes are formed at the plane different from the data lines.

10. A thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate;

a gate line assembly formed on the substrate and comprising gate lines, and gate electrodes connected to the gate lines;

a linear common electrode formed on the substrate and separated from said gate line assembly;

a gate insulating layer covering said gate line assembly and said common electrode;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes;

a light interception pattern formed on the gate insulating layer and of same material as the semiconductor pattern;

a data line assembly comprising a source electrode and a drain electrode formed on the semiconductor pattern, and data lines connected to the source electrode and crossing over the gate lines to define a pixel region; and

a linear pixel electrode formed at the pixel region and alternatively located side by side with the common electrode, wherein the pixel electrode is coupled to the drain

electrode.

11. The thin film transistor array substrate of claim 10, wherein the light interception pattern is overlapped with the corresponding data line, and the common electrode or the pixel electrode close to the corresponding data line.

12. The thin film transistor array substrate of claim 10, wherein the light interception pattern is overlapped with the common electrode or the pixel electrode of the neighboring pixel regions.

13. The thin film transistor array substrate of claim 10, wherein the semiconductor pattern is connected to the corresponding light interception pattern.

14. The thin film transistor array substrate of claim 13, wherein the semiconductor pattern is extended to the bottom of the corresponding data line.

15. The thin film transistor array substrate of claim 14, wherein the light interception pattern is extended external to the periphery of the data line.

16. The thin film transistor array substrate of claim 14, wherein the semiconductor pattern has the same shape as the data line except the channel portion between the source electrode and the drain electrode.

17. The thin film transistor array substrate of claim 10, wherein the pixel electrodes are formed at the same plane as the data lines.

18. The thin film transistor array substrate of claim 17, wherein the semiconductor patterns are extended to the bottom of the pixel electrodes.

19. The thin film transistor array substrate of claim 10, further comprising a protective layer covering the data line assembly and having contact holes

wherein the pixel electrode is formed on the protective layer and connected to

the drain electrode through the contact holes.

20. The thin film transistor array substrate of claim 10, further comprising an ohmic contact pattern interposed between the semiconductor pattern and the data line assembly.

21. The thin film transistor array substrate of claim 20, wherein the ohmic contact pattern has the same shape as the data lines.

22. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly and a common line assembly on an insulating substrate, the gate line assembly comprising gate lines and gate electrodes, and the common line assembly comprising common electrodes;

forming a gate insulating layer on the substrate covering the gate line assembly and the common line assembly;

forming a semiconductor pattern on the gate insulating layer;

forming a on the gate insulating layer light interception pattern of same material as the semiconductor pattern;

forming on the gate insulating layer a data line assembly comprising a source electrode and drain electrode, and data lines; and

forming a pixel electrode.

23. The method of claim 22, wherein the data line assembly is formed at the same plane as the pixel electrodes.

24. The method of claim 23, wherein the light interception pattern, the semiconductor pattern, the data line assembly and the pixel electrode are formed

through photolithography using a photoresist pattern.

25. The method of claim 24, wherein the photoresist patterns comprise a first pattern with a predetermined thickness placed at the channel portion between the source and the drain electrodes as well as at the light interception patterns, a second pattern having a thickness larger than the thickness of the first pattern, and a third pattern having a thickness smaller than the thickness of the first pattern.

26. The method of claim 25, wherein the photoresist patterns are formed using one mask.

27. The method of claim 26, wherein the steps of forming the semiconductor pattern, the light interception pattern, the data line assembly and the pixel electrode further comprise the steps of:

sequentially depositing a semiconductor layer and a conductive layer on the gate insulating layer;

coating a photoresist film onto the conductive layer;

exposing the photoresist film to light through the mask;

developing the photoresist film to form the photoresist patterns, the second photoresist pattern being placed over the data line assembly;

etching the conductive layer under the third photoresist pattern and the underlying semiconductor layer to from the semiconductor pattern and the light interception pattern;

removing the first photoresist pattern through ashing;

etching the conductive layer the second photoresist pattern as mask to complete the data line assembly and the pixel electrodes; and

removing the remaining photoresist pattern.

28. The method of claim 27, wherein the semiconductor pattern has the same shape as the data line assembly except the channel portion between the source electrode and the drain electrode.

29. The method of claim 28, wherein the light interception pattern, the semiconductor pattern and the data line assembly are formed through photolithography using a photoresist pattern.

30. The method of claim 29, wherein the photoresist pattern comprises a first pattern with a predetermined thickness placed at the channel portion between the source electrode and the drain electrode, a second pattern having a thickness larger than the thickness of the first pattern, and a third pattern having a thickness smaller than the thickness of the first pattern.

31. The method of claim 30, wherein the photoresist pattern is formed using one mask.

32. The method of claim 31, wherein the step of forming the semiconductor pattern, the light interception pattern, and the data line assembly further comprises steps of:

sequentially depositing a semiconductor layer and a conductive layer on the gate insulating layer;

coating a photoresist film onto the conductive layer;

exposing the photoresist film to light through the mask;

developing the photoresist film to photoresist patterns, the second photoresist pattern being placed over the data line assembly;

etching the conductive layer under the third photoresist pattern and the underlying semiconductor layer to form the semiconductor patterns and the light interception patterns;

removing the first photoresist pattern through etch back, and etching the second photoresist pattern;

etching the conductive layer using the second photoresist pattern as mask to complete the data line assembly; and

removing the remaining photoresist pattern.

33. The method of claim 32, wherein the pixel electrodeis formed at the plane different from the data line assembly.

34. The method of claim 33, further comprising the step of forming a protective layer after forming the data line assembly to cover the data line assembly; and

forming the pixel electrodes being formed on the protective layer.